INTEGRATING CHIPUS BATTERY CHARGER IPS INTO YOUR SOC AN-1711

1 Features

- Configurable charge current (10mA to 1.5A)
- Integrated power FET and sensing
- Trickle, fast, and constant voltage charging modes
- Integrated protections (temperature, voltage and reverse current)
- Charging status flags
- Digitally programmable parameters
- USB compatible

2 Applications

- Portable devices SoCs / PMICs
- Tablet PCs / Smart phones
- PDAs / Handhelds

3 Introduction

As time-to-market and risk reduction become crucial, the use of semiconductor intellectual property (IP) blocks enable the fast design of successful integrated circuits (ICs) and systems on chips (SoCs). Observing the trend in portable electronic devices and Internet of Things (IoT), Chipus has developed a family of linear battery charger IPs (CM1711ff, CM1712ff, CM1713ff) targeting single cell Li-Ion batteries. This kind of battery is widely used in cellphones, tablets, readers, medical devices, cameras to name a few applications. In modern mobile applications, both physical size and cost are important characteristics of the end product. Integrating the battery charger into an SoC not only reduces the bill of materials (BoM), but also cut printed-circuit board (PCB) area.

All Chipus battery charger IPs are monolithically integrated including all voltage, current and clock references needed for proper operation. With output voltages ranging from 3.3V to 4.35V, these IPs are suitable for portable applications and easy to be integrated into SoC solutions. They are capable of charging from an AC adapter or USB, also featuring backup charger and several built-in protections. Integrated NTC for battery pack temperature control is included in CM1711ff and CM1713ff, but can easily be added to CM1712ff upon request.

This application note briefly describes Chipus family of battery charger IPs and discusses a typical case of use. For more information about specifications, IP list and news, visit www.chipus-ip.com.

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4 Overview of Chipus Battery Charger IPs

The simplified block diagram of Chipus battery charger IPs including connections to external components is shown in Fig. 1. The power switch is an integrated PMOS device able to provide up to 1.5A in fast charge mode. Using a digital interface or simple external resistors, the IPs can be configured to provide a charge current from 10mA to 1.5A. The CM1711ff also provides an auxiliary output to charge a backup coin battery responsible for critical functions such as real time clock.

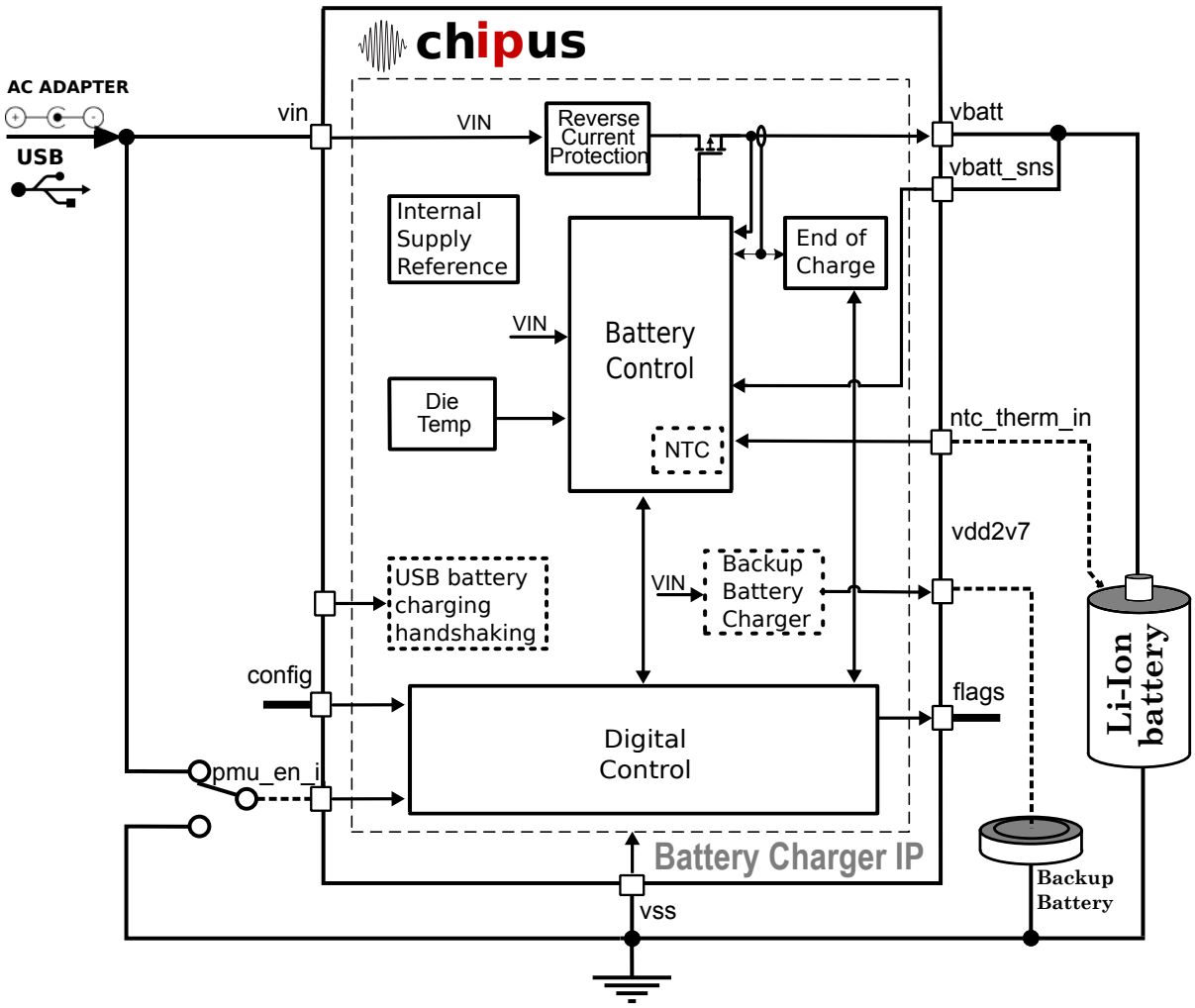

Fig. 1. Simplified block diagram for Chipus battery charger IPs.

Observing best practices when dealing with Li-ion batteries, these IPs feature 3 charging modes: trickle current (used when the battery presents extremely low voltage), fast mode (ordinary charging mode providing up to 1.5A) and constant voltage mode (used when battery is almost full). The charge modes

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are automatically controlled and the IPs provide information about the charge process, such as the “end of charge” flag, through its digital interface.

The IPs include all necessary voltage, current and clock references that are needed for the correct operation, thereby simplifying integration into SoC applications.

Other functions such as die temperature and current sensing are implemented to protect the battery charger itself and to avoid damages to the end product. The “End of Charge” circuit senses the output current and turns off the charger when battery is full. If die temperature rises above safe levels, the charger is also disabled. Reverse current protection is implemented to avoid the battery from discharging in case the input voltage drops below the battery voltage or an accidental short circuit takes place. Dashed blocks in Fig. 1 are not present in all IP versions.

A comparison of the features of the different battery charger IPs provided by Chipus is presented in Table 1.

Table 1: Comparison among battery charger IPs from Chipus.

Feature	CM1711ff (Silicon Proven)	CM1712ff (Silicon Proven)	CM1713ff (Under Development)
Termination voltage (V)	4.2	4.2	3.3 — 4.35 (configurable)
Termination voltage accuracy (%)	± 1	± 1	± 1
Input operating voltage range (V)	4.5–5.5	4.5–6.9	3.3–6.9
Absolute maximum input voltage (V)	5.5	30	22
Charge current range (A)	0.1–1.5	0.1–1.1	0.01–1.1
Configurable charge current	Yes (digital)	Yes (external resistors)	Yes (digital and external resistor)
Battery leakage current (μA)	3.2	1	4.2
Consumption in sleep mode	–	–	tens of nA
Integrated power FET and sensing	Yes	Yes	Yes
Built-in NTC	Yes (with internal resistor)	No	Yes
Backup battery charger	Yes (ML series, 3mA)	No	No
Charging status flags	Yes	Yes	Yes
Under / Over Voltage Protection	Yes	Yes	Yes

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Table 1: Comparison among battery charger IPs from Chipus.

Feature	CM1711ff (Silicon Proven)	CM1712ff (Silicon Proven)	CM1713ff (Under Development)
Internal voltage, current, and clock refs.	Yes	Yes	Yes
Reverse current protection	Yes	Yes	Yes
Over temperature protection	Yes	Yes	Yes
Off battery detection	Yes	No	Yes
Fast charge mode timeout	No	No	Yes (7h)
USB compatible (100mA / 500mA)	Yes	Yes	Yes
USB battery charging handshaking	No	No	Yes
Serial Interface (m bits)	–	$m = 4$	$m = 2^*$
Digital interface (n bits)	$n = 19$	$n = 70$	$n = 188$
OTP memory	No	Yes	Yes*
Process technology	0.18µm CMOS (SilTerra C18GH5)	0.18µm BCD (SilTerra D18V)	0.18µm BCD (SilTerra D18V)

* Licensable as a separate IP.

5 Typical Case of Use

As the presented battery charger IPs include all references that are needed for correct operation, it is simple to integrate them in an SoC. Because of the large charging current, care with electromigration and excessive voltage drop issues must be taken when connecting both “vin” and “vbatt” pins.

Fig. 2 illustrates how a battery charger IP can be integrated in a SoC for a battery powered application.

5.1 Power Signals

In order to handle the charge current provided by the IP, it is important to draw metal tracks and choose the number of pads properly. For large charge current, such as 1.5A, the use of 3 pads in parallel is recommended for both “vin” and “vbatt” pins. Thick metal tracks (preferably using a sandwich of 3 metal layers) and 3 bondwires in parallel guarantee the current handling capability without reduction in the product

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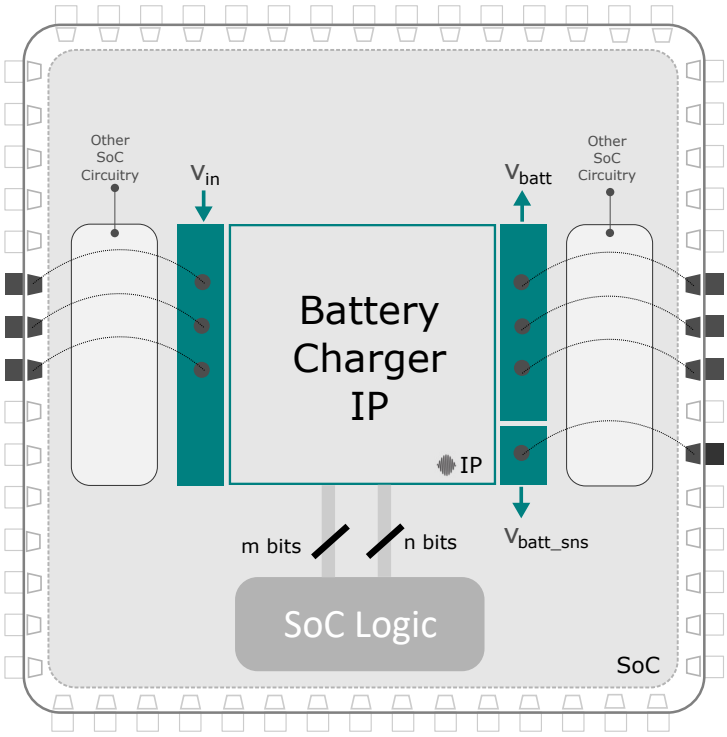

Fig. 2. Integration of battery charger IP in a SoC.

lifetime. In case the IP is placed far from the die edges, other SoC circuitry can be placed below the bondwires as depicted in Fig. 2. If this is not possible, the sandwich of 3 metal tracks can be extended to the edge of the SoC connecting directly to the pad ring and then, with short bondwires to the IC package leadframe.

The closed loop operation requires that the battery voltage is sensed physically as close as possible to the battery to avoid unwanted voltage drop that might alter the sensed battery voltage. Special care with this signal must be taken as the precision of the IP depends on the proper assembly.

5.2 Digital Interface

Integrating a battery charger IP also requires that the IP is able to properly communicate with the main logic of the SoC. For this purpose, it is necessary to route a digital bus between the battery charger IP and the main processor. The bus size depends on the actual chosen IP and values are presented in Table 1. Not all signals of the digital interface are required to be connected.

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5.3 Serial Interface

Specifically, for CM1712ff, a 4-bit serial interface is available to configure the IP. This configuration can be made either by the SoC main logic or externally. For the other battery charger IPs, a separate serial interface IP can be licensed separately and integrated upon request.

5.4 The IP integrated in a testchip

Emulating the application shown in Fig. 2, the CM1711ff battery charger IP was implemented in a test chip for characterization purposes. A photograph of the testchip die is shown in Fig. 3. As expected, a large portion of the IP is consumed by the power MOSFET.

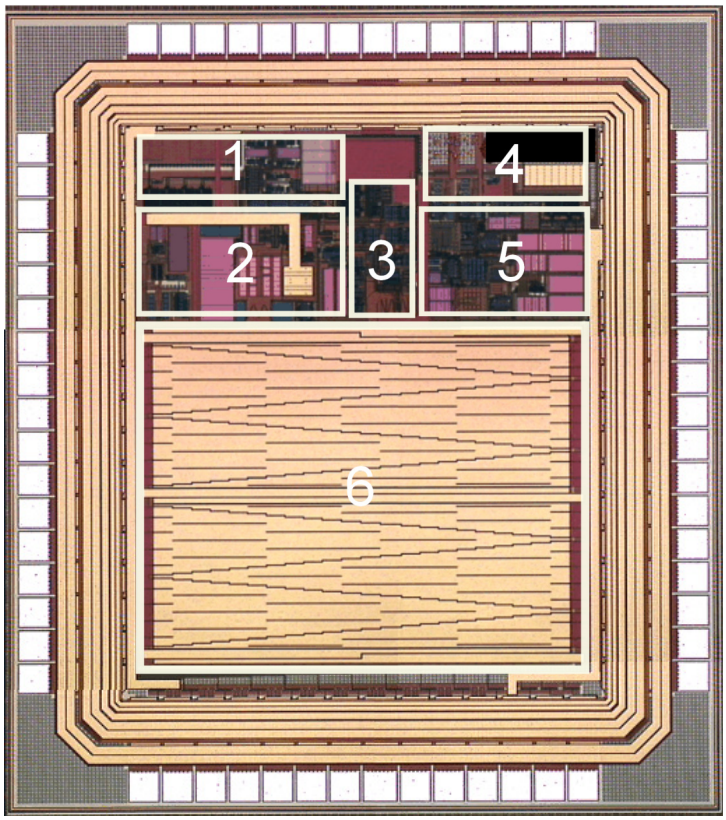

Fig. 3. CM1711ff die photograph.

The charging behavior of a 2400mAh battery is shown in Fig. 4. For this measurement, the full charge current of 1.5A was used. In Fig. 4, all charging modes can be observed. In the beginning of the charge, battery voltage was low, which triggered trickle current mode. As the battery voltage rises, fast charge mode is enabled and charge current reaches 1.5A and it is kept constant until the battery achieves 4.2V. At this

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moment, the charger switches to constant voltage mode and battery current is reduced as time passes. Around 3 hours after charging has started, battery current has dropped below 10% of maximum current and the battery charger assumes the battery is full. At this moment, battery current is cut and the end of charge flag rises to logical “1”.

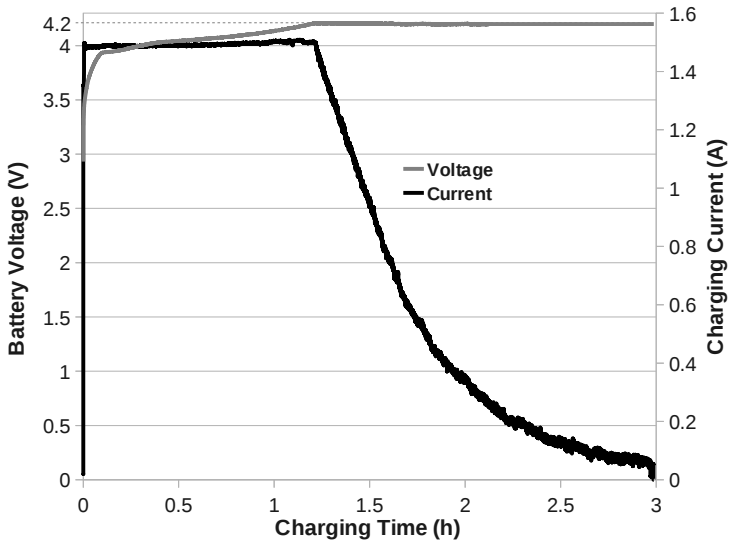

Fig. 4. CM1711ff current and voltage charge profile.

6 Conclusion

Providing battery charging capabilities to your SoC is an important differentiator and it enables a set of innovating and successful products that follow the modern mobile trend. All the battery management is made automatically by the IP and only ordinary digital control bus from the main logic is needed to integrate this IP into the final SoC.

This document provided basic information about battery charger IP family developed by Chipus and how to integrate them into your SoC. For further information, please write to ip@chipus-ip.com and visit us at www.chipus-ip.com.

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About Chipus

Chipus Microelectronics (www.chipus-ip.com) is a semiconductor company focused in the development of low-power, low-voltage, analog and mixed-signal intellectual property (IP) blocks for integrated circuits (ICs) and systems on chip (SoCs).

Relying on a strong experience in power management and data converters, the company has more than 150 IP blocks in process nodes from 40nm to 0.35um of various foundries. Since its foundation in 2008, Chipus has licensed such IPs and provided associated IC design services with firm commitment and flexible client support to customers worldwide (South and North America, Europe, and Asia).

Headquartered in Florianópolis, Brazil, Chipus has a US subsidiary in Silicon Valley and sales teams in both USA and Europe. For further information, do not hesitate to contact us at ip@chipus-ip.com.

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