ANALOG IC
LAYOUT
SERVICES

INTEGRATING IDEAS. INSPIRING PEOPLE.

Bringing your ideas to life with our designs.
Providing world-class services and customer support.

www.chipus-ip.com

chipus

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ounting on an experienced design team and almost 10 year of track record with customers around the world, Chipus has developed a large analog intellectual property (IP) portfolio in technologies from 0.35μm down to 40nm.

The knowledge and experience accumulated along these years enables us to assist semiconductor companies to successfully launch their innovative products in the market on schedule.

This document describes how Chipus is able to support you in **analog integrated circuit (IC) layout** leading you through our business model, presenting what inputs we expect from you and what outputs you may expect from us. We also present some success cases to give you confidence that you have found the right partner.

IC Layout Expertise

**General IC Design:** Since its inception in 2008, Chipus has been working in complex IC designs, applying thorough verification with demanding customers around the world. As a result of years of work, Chipus has built a wide IP portfolio that spans from true ultra-low-power (ULP) references up to 1.8A power management circuits, high resolution ADC and DACs, sensor interfaces, and RF front ends to name a few.

**Analog Layout:** Chipus is able to deliver high quality analog IC layout for different applications in semiconductor design with the following expertise:

- **Low power circuit design**
- **Low noise circuits**
- **Sensitive analog front-ends**
- **Mixed signal designs**
- **Proven RF capabilities**
- **Metal-fix strategy**
- **Spare-cells strategy**
- **Third part IPs integration**

- **Experience with automotive layout**
- **Experience with BCD technologies**
- **High current power management**
- **High current power devices**
- **MIxed signal IO integration**
- **ESD-aware design**
- **Latch-up-aware design**
- **Electromigration-aware design**
- **Thermal dissipation-aware design**

With our layout expertise and proven experience with CMOS and BCD technologies in nodes from 0.35μm down to 40nm of leading foundries such as TSMC, Global Foundries, XFAB,

TowerJazz, Silterra, AMS, and others, we are able to deliver best-in-class full-custom IC layout services.

Physical Verification: DRC, LVS, ERC, and antenna are always verified for all circuits layouted by our team.

Parasitic Extraction: according to customer requirements, Chipus can provide the schematic back-annotated with parasitics extracted from layout.

Design Complexity: Our technical team is qualified to work with both simple building blocks and complex chip level designs, being able to provide a verified layout database or GDSII to be integrated into your SoC or a full chip GDSII ready to be taped out.

ASICs: we have proven experience in delivering full custom IC designs for our customers, which requires expertise to:

- intelligent floorplanning with attention to sensitive blocks, tracks, and temperature gradients;
- build IO pad ring, with special attention to foundry rules for voltage supply pads distribution and mixed digital and analog IO cells;
- deal with multiple supply voltage domains;
- add sealring, dummy metals, dummy diffusion, and dummy poly;
- prepare GDS and tape-out forms for MPW and MLM runs;
- plan reticle for MLM and single mask runs.

EDA: Our team has experience with Cadence and Synopsys tools for analog IC layout design and Mentor Calibre is our main physical verification tool for signing off all our layouts.

Semiconductor Physics and Fabrication Process: Chipus layout team is composed of Electrical and Computer Engineers with background in analog IC design, and, hence, have a very good understanding of the transistor operation, semiconductor physics, and the IC fabrication process.

Confidential Information

Chipus treats customer information with the same care it handles its own. We take special care in keeping information contained and our technical team is used to working under these conditions.

As our main goal is to build long-term relationships, it is important for us that trust is built. Technical details, business strategies and decisions will not leave Chipus premises.

We normally use our SFTP server to exchange project files and documents with our customers, ensuring a secure transfer of sensitive information.

Your Layout Project

As matter of quality assurance, evidenced by our **ISO 9001:2015 certification**, layouts made by Chipus follow the flow shown below (Figure 1). Chipus IPs go through the exact same process ensuring high quality designs. Our layout team is always driven by the highest quality standard in all projects they take in.
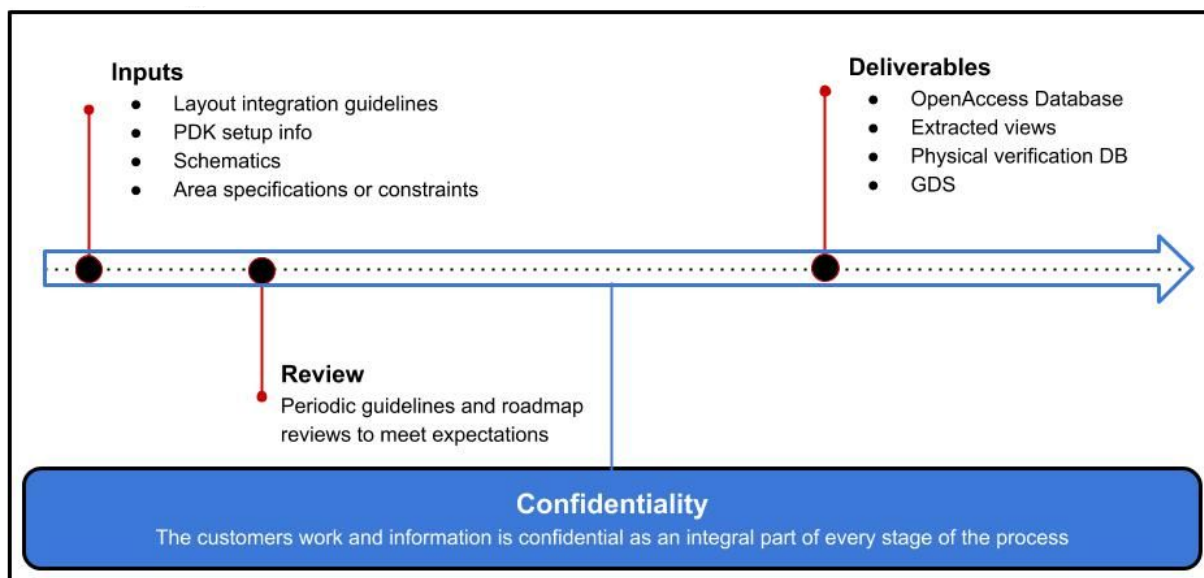

Figure 1: Chipus Layout project phases.

Chipus divides the layout project in the following phases:

1. **Inputs From Customer**

2. **Reviews**

3. **Delivery**

As it was mentioned before, **confidentiality** is an integral part of the process and maintained as a base throughout all its phases. Let us describe in deeper detail what consists each step, its inputs and outputs and how it affects the progress of the project.

1. Inputs From Customer
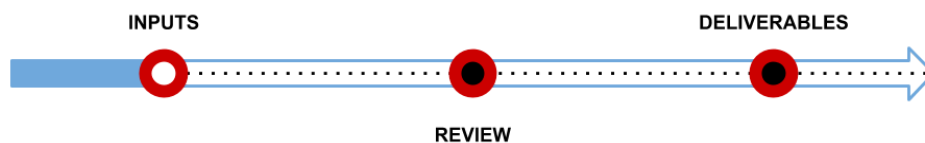
Besides all technical inputs that are required (PDK setup info, schematics, area specifications or constraints) it is often necessary to discuss other actions associated with business and technical details that must be taken before the start of the project. Below, we comment the most important ones.

1.1.   Business Model

From our experience, companies often decide to outsource layout when they notice that they will have problems keeping the schedule. In situations such as this, fast planning and decision making are mandatory. Chipus is used to this kind of situation and we are able to start the project right after the paperwork is completed, which can be done in a couple of days.

After taking the decision of involving Chipus in your challenge, the first step is to decide the most appropriate business model for you. Each customer has its own criteria and Chipus generally works with:

1. **Fixed cost**

As the name itself implies, a fixed fee applies for the given project which minimizes the risk for the customer. A fixed cost approach requires that a project leader from Chipus project is involved up front to estimate the size of the project. This step is fast and often can be done in a few days. This celerity is essential to keep up the schedule of the project.

2. Time and materials

This approach provides more flexibility for projects with specifications prone to modifications with need of reiterative feedbacks. This approach basically adds resources to your layout team and this additional resource can be in close cooperation with the existing team to ensure efficient progress.

1.2. EDA Licenses

Chipus normally incorporates EDA license fees into its service offering. Nevertheless, Chipus has also had successful experiences using customers' infrastructure both remotely and locally (at the customer site).

1.3. Integration Guidelines

Integration guidelines are requested by Chipus before the beginning of the project to increase efficiency and reduce the need for unnecessary discussions with the customer. If there are no specific guidelines from the customer, Chipus will employ its own set of layout guidelines to ensure that layout best practices are observed.

1.4. Acceptance criteria

Continuous and efficient communication is our main design tool. At the beginning of the project we will decide the end of project and acceptance criteria along with the customer so that all expectations are met.

2. Reviews

Each company has design guidelines that they use to ensure quality of their own products. Such guidelines vary for different circuits: a common building block such as a variable gain amplifier will use different layout techniques if it is targeted for low noise, high bandwidth or high accuracy.

In order to ensure that the layout drawn by Chipus captures the design requirements demanded by circuit designers, we often apply frequent design reviews and an intensive (yet efficient) communication with the customer.

Our layout team has worked in extreme situations where time constraints left no place for mistakes and short reviews were made on a daily basis. On the other extreme, we have worked with customers that requested only one design review before project acceptance. Another solution already adopted in some projects was to send out the technical team to the customer's site to improve communication and speed up project schedule.

3. Deliverables

At the end of the layout project, we deliver to the customer:

1. **Complete open access database**
2. **Extracted views for verification with layout parasitics**
3. **Physical verification database**
4. **GDS**

Other deliverables may be prepared upon request.

Digital Back-end

Although it is not the focus of this document, it is important to mention that Chipus is also able to implement digital back-end. This capability enables us to work with more complicated mixed signal designs or fully digital designs.

Chipus has worked with complex digital implementation in technologies down to leading edge 7nm process featuring around 2.5M placeable cells.

Integration of analog and digital sections can be made both using analog-on-top or digital-on-top approaches. This depends only on the complexity of the overall design and it is decided case by case.

Why work with Ch**ip**us?

- Chipus works closely to your design team with efficient and continuous communication
- Chipus has an experienced team of motivated semiconductor experts and enthusiasts
- Chipus is almost 10 years in the market with customers in North and South America, Europe, and Asia
- Chipus is able to support you in your design, either in the development of small building blocks or in the top level integration of complex chips
- Chipus offers flexible EDA licensing schemes
- From top management to technical team, Chipus is concerned with confidentiality
- Chipus is ISO 9001:2015 certified

Not convinced yet? Please, check some **success cases** in the last section of this document and/or schedule a meeting with us.

Full-Custom IC Layout Services Testimonials

Here are some words from customers who valued our service and our Layout Services specifically. See what they have to say about Chipus' services and our team.

"Chipus' layout work was performed with high quality and in shortest time and all our requirements and wishes were fulfilled".

Head of Analog and Mixed-Signal Systems Group

Renowned German Research Institute

"We have a long-term cooperation with Chipus regarding mixed signal design projects. Chipus helped us out to compensate lacking resources in analog & digital circuit design, manual chip layout and verification. I can only say that Chipus is a reliable partner with excellent technical skills and helped us a lot to deal with the requirements of our demanding and fast changing market today"

Chief Executive Officer
**ASIC Company based in Germany
with strong emphasis on automotive
and industrial applications**

IPs and ICs Success Cases

Chipus has developed analog integrated circuit layout for its whole IP portfolio and for the ICs and testchips it has integrated in its almost 10 years in the market. Our layout capabilities are proven by the successful products that our ASICs and IPs enabled worldwide.

The cases presented here were chosen to demonstrate our layout expertise in different fields of analog IC design such as:

- **Analog front-ends for sensitive signal acquisition**
- **Custom analog-front ends**
- **Power management circuits with high current handling capabilities**
- **Ultra low power circuits**
- **RF front-ends**

Low noise amplifier for neural sensors IC

This design is a low noise amplifier for acquisition of neural signals which are known to be very sensitive to noise due to their very low amplitude characteristics.
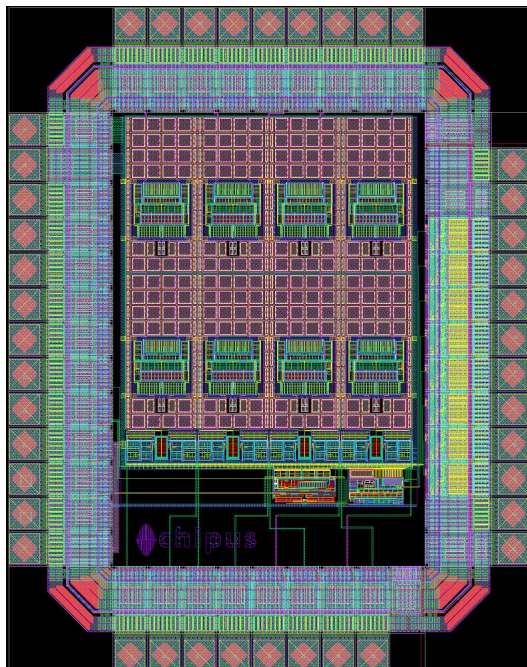
The front-end was designed to match the impedance of the Silicon Carbide (SiC) electrodes, thus enabling better neural compatibility of the entire system. Each stage is capacitively coupled to reduce the offset around the common mode reference.

Layout technique highlights:

- Low noise
- Fully differential
- Ultra low power
- Intricate matching scheme

The IP core is a 2-stage, 46-dB, fully-differential amplifier featuring low noise and ultra-low-power consumption. It was designed in SilTerra 0.18μm CMOS technology. This circuit is silicon proven and measurements are available upon request.

USB/AC Li-Ion battery charger IPs

These IPs are targeted to SoCs that are used in mobile products such as smartphones, tablets, and wearables. They were designed for SilTerra 0.18μm CMOS and BCD technologies.
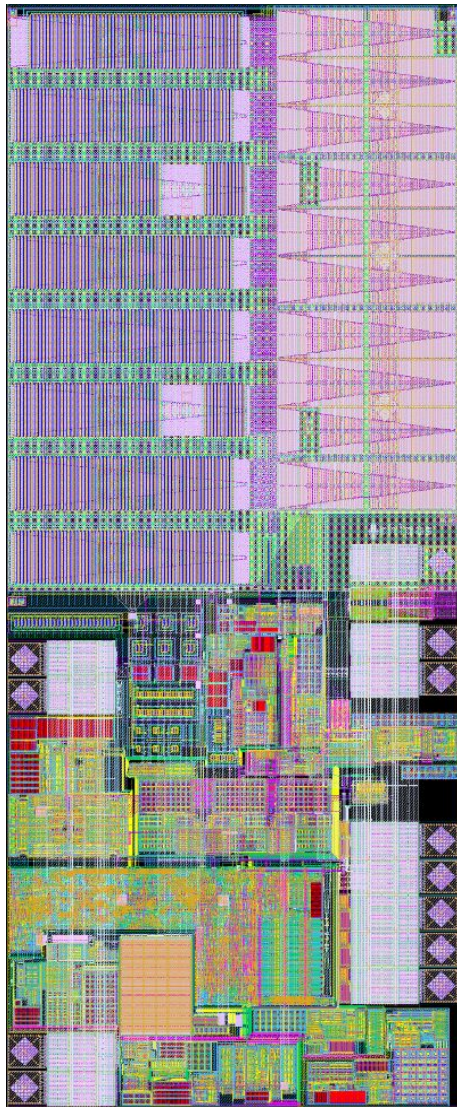
In order to enable charging mode, the IP senses the temperature of the die, the battery voltage and the supply voltage. Temperature, over voltage and reverse current protections are implemented to ensure safe operation of the battery.

Battery lifetime in maximized with charging modes that are automatically selected depending on battery voltage. If battery voltage is too low, trickle charge is enabled: in this mode a small current is used to charge the battery slowly. When battery voltage is in a safe region, maximum current is enabled. When terminal battery voltage is achieved, the charger is turned into constant voltage mode until the battery is fully charged. Current is completely cut once the battery is charged.

Layout technique highlights:

- High current (up to 1.8A)
- High voltage (up to 30V tolerant input)
- DMOS transistors
- Mixed signal design
- Trimmable

These IPs deal with a current of up to 1.8A and special layout techniques were used to ensure both low drop in the metal tracks and robustness. The newest member of this IP family (CM1713ff) has built-in USB detection for charging applications and the input is able to deal with up to 22V.

All battery charger IPs are silicon proven and the latest version has been integrated in a power management integrated circuit (PMIC) for an european customer that is planned to enter volume production until the end of 2018.

Full UHF RFID EPC Class 1 Gen 2 and ISO 18000-6C passive tag IC
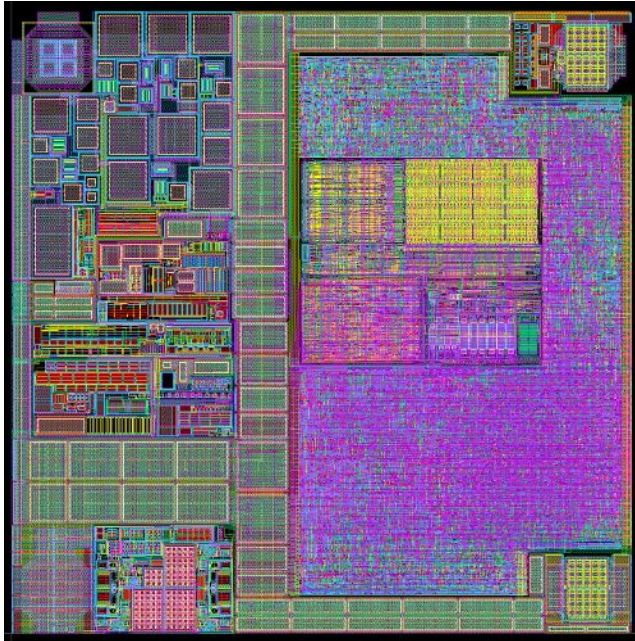
This ASIC is a complete UHF (860MHz - 960MHz) RFID passive tag IC that implements EPC gen 2 protocol in SilTerra 0.18μm CMOS. It consists of three main blocks: **i)** analog/RF front-end, **ii)** digital baseband processor, and **iii)** non-volatile memory (NVM).

The analog/RF front-end (CM9011ff) is responsible for harvesting energy from an RF signal emitted by an RFID reader, limiting the input voltage if the RF power is too high, and for implementing the backscatter communication. Measurements of the RFID tags built with this ASIC, whose main design target was area reduction, have shown a read sensitivity around -12dBm. The chip features a ULP PMU with a power-on reset (POR) circuit, oscillator and current/voltage references.

Digital baseband RTL was licensed from third party and digital backend was implemented at Chipus with power optimizations that led to approximately 30% reduction in power. The NVM was licensed from Synopsys and this success case has been reported in Synopsys website.

Chipus has also worked in the design of another RFID tag IC for a Chinese customer to comply with Chinese RFID standard (GB standard). This improved RFID ASIC has attained a measured read sensitivity of -17dBm.
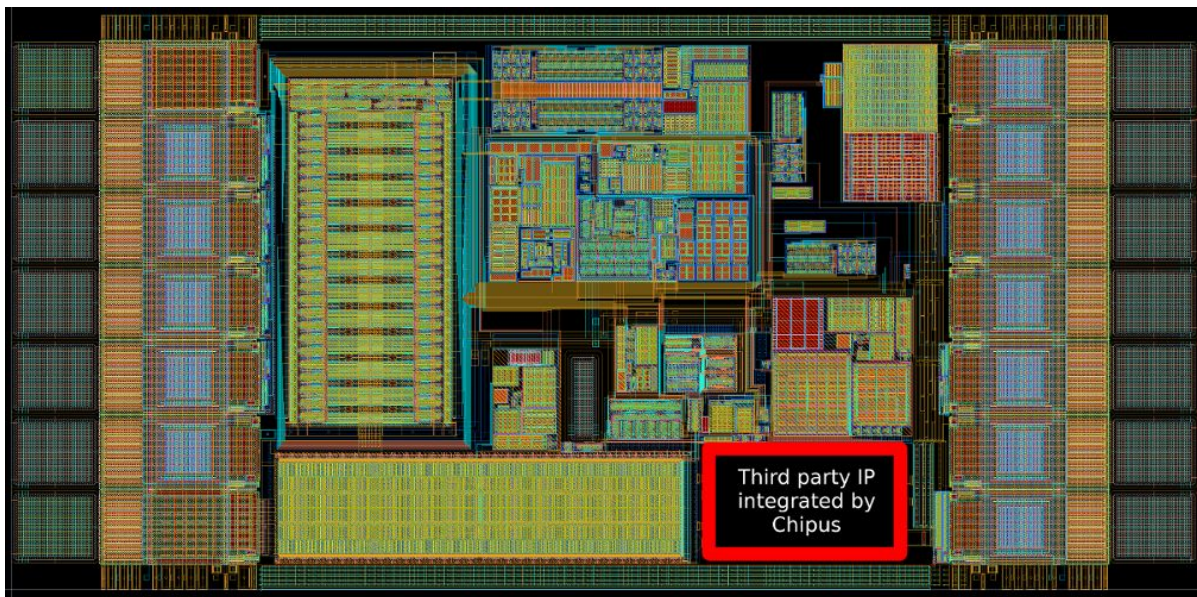
Layout technique highlights:

- RF design up to 1GHz
- Ultra low power
- Mixed signal project

- Integration with third-party IP in ASIC
- Trimmable

Custom ASIC for magnetic sensor

This project consisted on the development of an ASIC for a custom magnetic switch sensor. The customer had developed an innovative magnetic sensor device, based on magnetic tunneling junction (MTJ) effect, and Chipus developed the ASIC to turn that innovative sensor into a product. This ASIC implements two types of switches for unipolar and omnipolar modes of operation. The unipolar switch senses external magnetic field in one direction while the omnipolar version allows to sense in both directions in the same axis.

The intensity of magnetic field that triggers the switch is configurable through adjustment of internal bias circuits parameters made during Factory Test Mode. This ASIC consists of **i)** a custom analog front-end, **ii)** an ultra-low-power PMU, **iii)** LED drivers, and **iv)** an OTP fuse memory for production trimming purposes.

This ASIC was developed in TowerJazz 0.13μm CMOS technology. Chipus is a featured TowerJazz IP partner.

Layout technique highlights:

- Interface with custom sensor
- Mixed signal project
- Integration with third-party IP (MTJ sensor device) in ASIC
- Trimmable

This ASIC is in volume production and it is a successful product developed in close partnership with the customer.

Galvanically isolated shunt current measurement system

This ASIC was designed for measuring shunt current of high voltage (5kV) power lines. The system is galvanically isolated and power is transmitted using inductive link integrated in a System in Package (SiP). It is designed in TSMC 0.18μm and it is now under measurements.
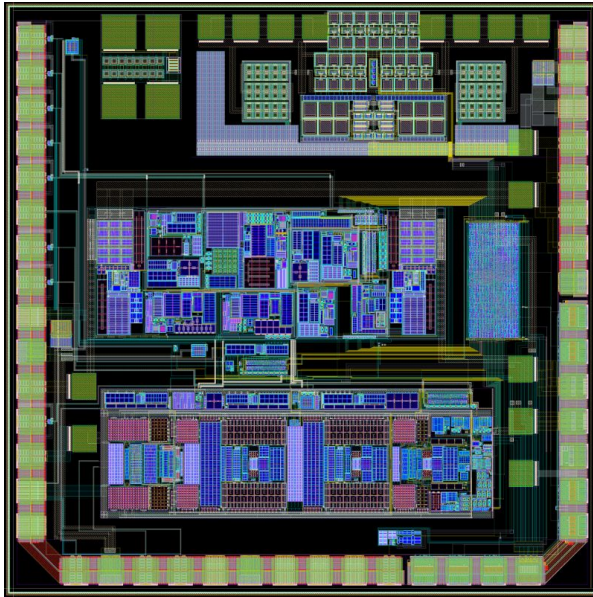
Chipus was responsible for the complete specification, design, verification and layout of the chip.

The ASIC features: **i)** integrated RF rectifier and RF power amplifier, **ii)** a linear power management unit (PMU) and **iii)** continuous time 3rd order 64MHz sigma-delta modulator, **iv)** analog and digital debug interface.

As power is transmitted through an inductive link, the rectifier must be able to deal with 25dBm generating an unregulated DC voltage that varies from 2V up to 3.6V. The PMU is responsible for generating 1.8V regulated voltage in both analog and digital power domains, generate voltage and current references and 64MHz clock signal that will be used by the sigma-delta modulator to sample the input signal. The sigma-delta modulator is sampled at 64MHz and achieves 13 bits ENOB (in simulation) with 50kHz input bandwidth.

Layout technique highlights:

- 2.4GHz RF power transfer
- Different analog power domains
- Integrated high-accuracy ADC
- Trimmable

Foundries

Chipus has close contact with several foundries and is eager to start new cooperations.

About Chipus

Chipus Microelectronics (www.chipus-ip.com) is a semiconductor company focused in the development of low-power, low-voltage, analog and mixed-signal integrated circuits (ICs) and systems on chip (SoCs).

Relying on a strong experience in power management and data converters, the company has more than 150 intellectual property (IP) blocks in process nodes from 40nm to 0.35μm of various foundries. Since its foundation in 2008, Chipus has licensed such IPs and provided associated IC design services with firm commitment and flexible client support to customers worldwide.

Headquartered in Florianópolis, Brazil, Chipus has a US subsidiary in Silicon Valley and sales teams in Brazil and Europe.

Bring your challenge to us! Write to services@chipus-ip.com and you will be contacted shortly by an engineer that will be able to understand your need and give you the appropriate support.

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